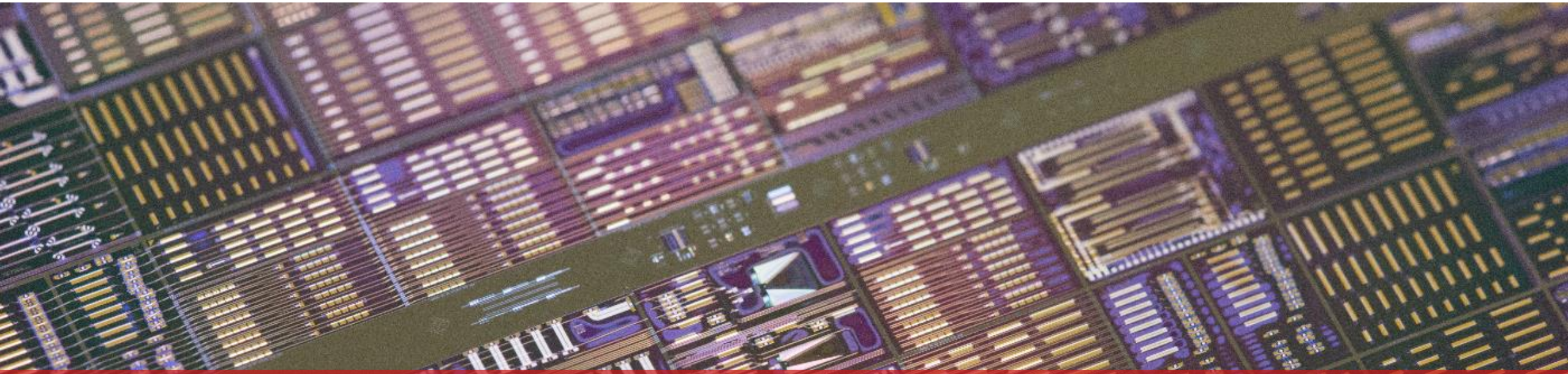
JENOPTIK

MORE LIGHT

Just the right PIC – How advanced test concepts enable fast PIC wafer-level tests

Tobias Gnausch | Sylwester Latkowski

13-03-2024



Electronic-Photonic Test Roadmap for Integrated Photonics

Jenoptik Webinar 2024

Sylwester Latkowski

Outline

- **Integrated Photonics**
  - Wind of the future and some challenges
- **Electronic-Photonic test for Integrated Photonic Systems**
  - Needs, challenges, and a crystal ball
- **Photonic Integration Technology Center**
  - Metrology Program at a glance

Photonics is all around round

- Tele-communications
- Data–communications

- Access to information
- Streaming
- Gaming
- Socializing
- Banking
- Trading
- Security

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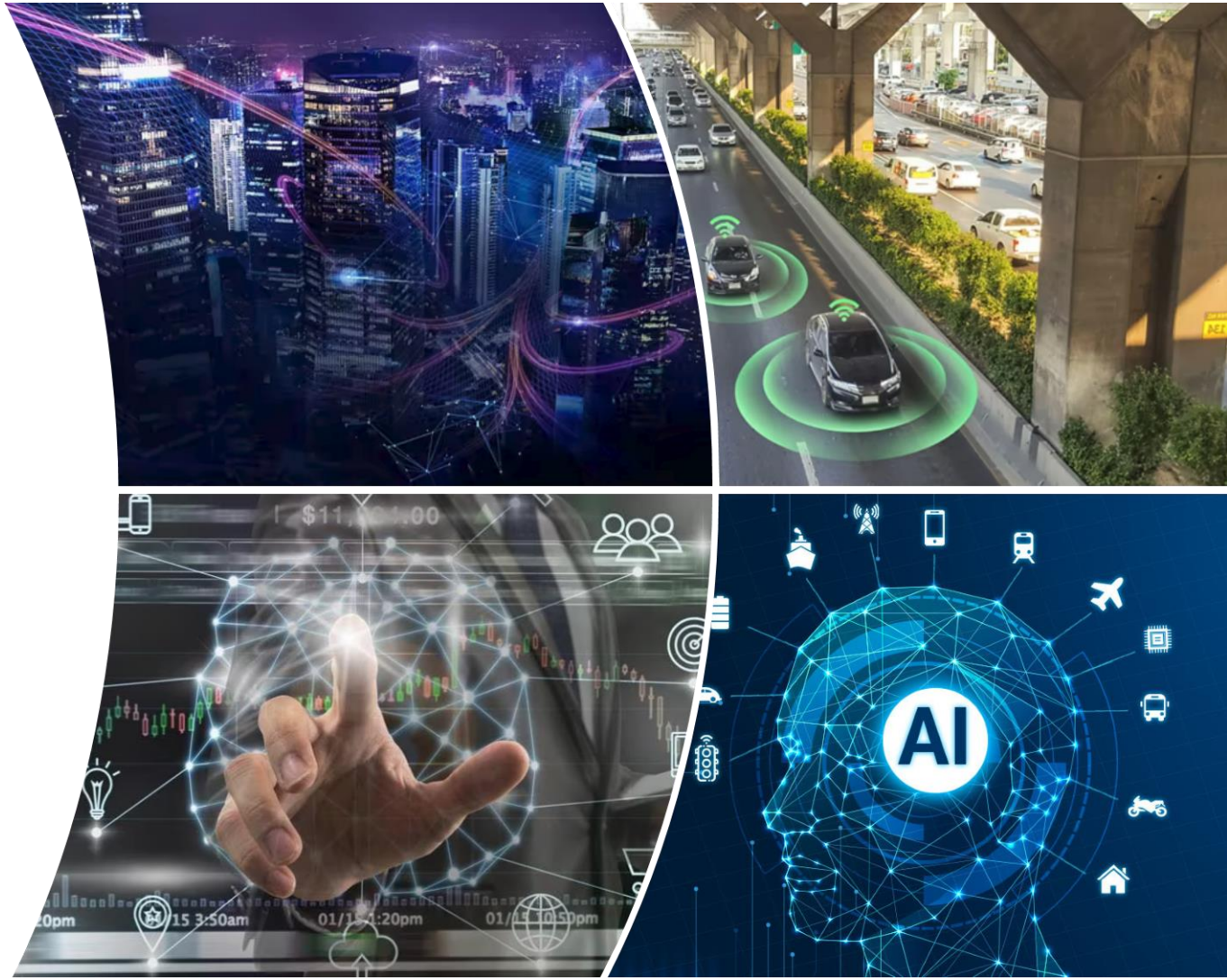
Even more photonics in the future

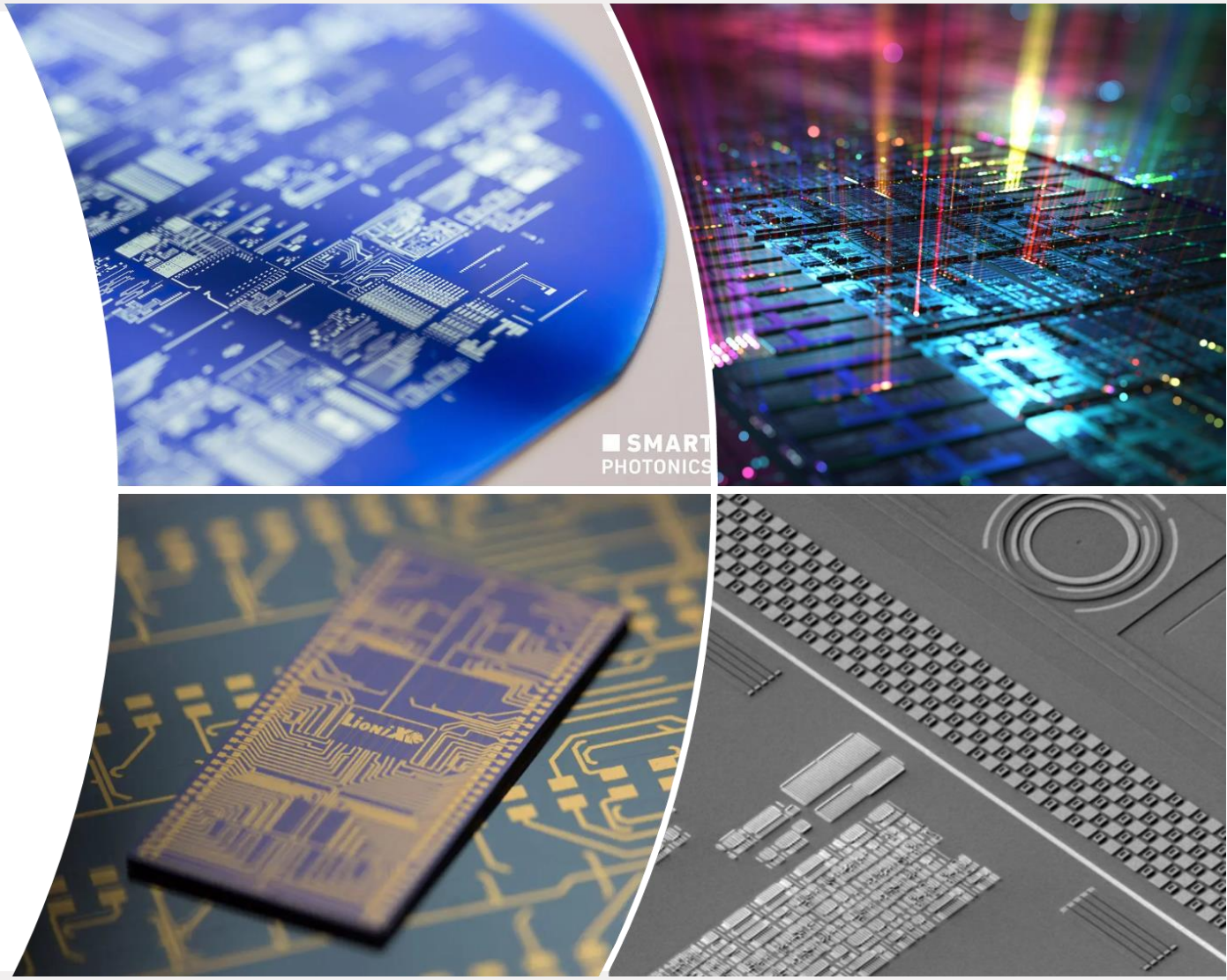
- Artificial Intelligence
- Quantum applications
- Autonomous transportation
- Sensors everywhere



Integrated Photonics System on a Chip

- Complex functionalities integrated
- Monolithic technologies
- Heterogeneous technologies

- No single one that suites all
- No real standards



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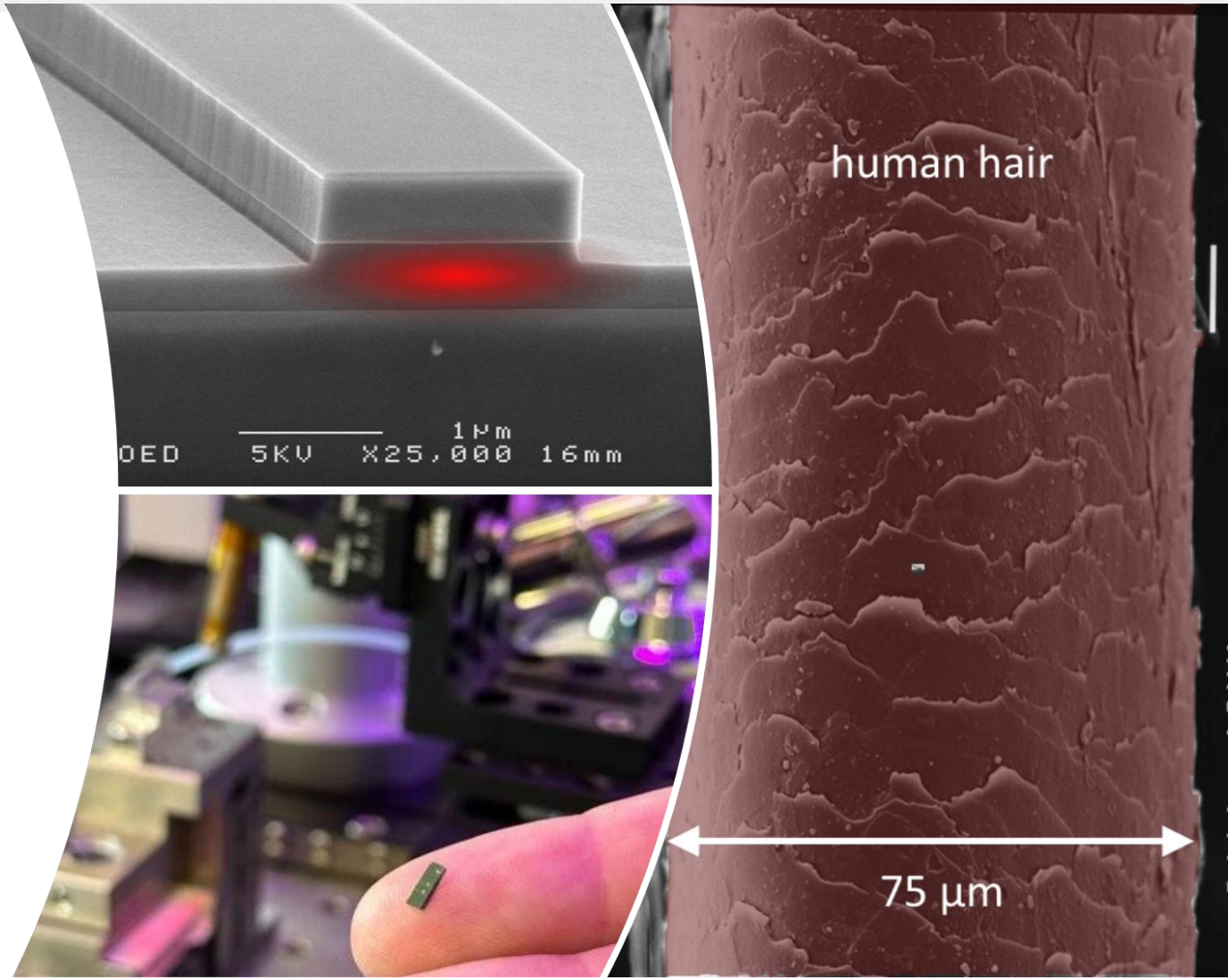
Integrated Photonics can be tiny

- Optical waveguides are in the micron
- Multi-IO systems are essential
- Several today -> Hundreds soon
- High-density optical IOs

- Optical alignment challenging
- Probing is challenging
- No standard IOs on the PIC side



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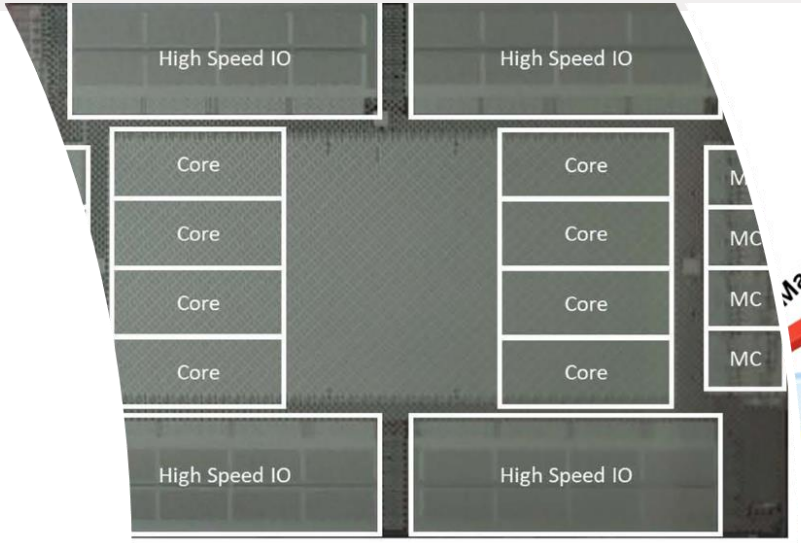
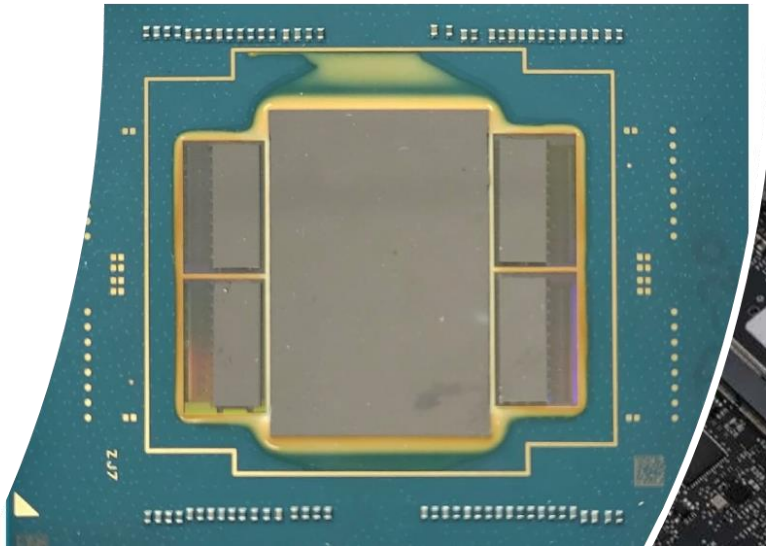
Photonics meets microelectronics

- Electronic-Photonic SoC
- Economy of scales
- Production at volumes

- High throughput test solutions
- Automated Test Equipment
- Highly parallel testing
- Electronic-Photonic Probing
- Standardization





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Electronic-Photonic Test

IPSR INTERNATIONAL

Driving Photonics Manufacturing

Role and importance of PIC testing

- Identify known-good-die (KDG)
- Push the performance-yield envelope
- Create improved accuracy models for the designers to make next generation product
- Testing is often a short-hand for
  - **Validation**
  - **Verification**
  - Selection
  - Measurement
  - Characterization

Ignazio Piacentini, Ficontec @ ECOC 2019:

„Validation: Do we make a right product?"

„Verification: Do we make a product right?"

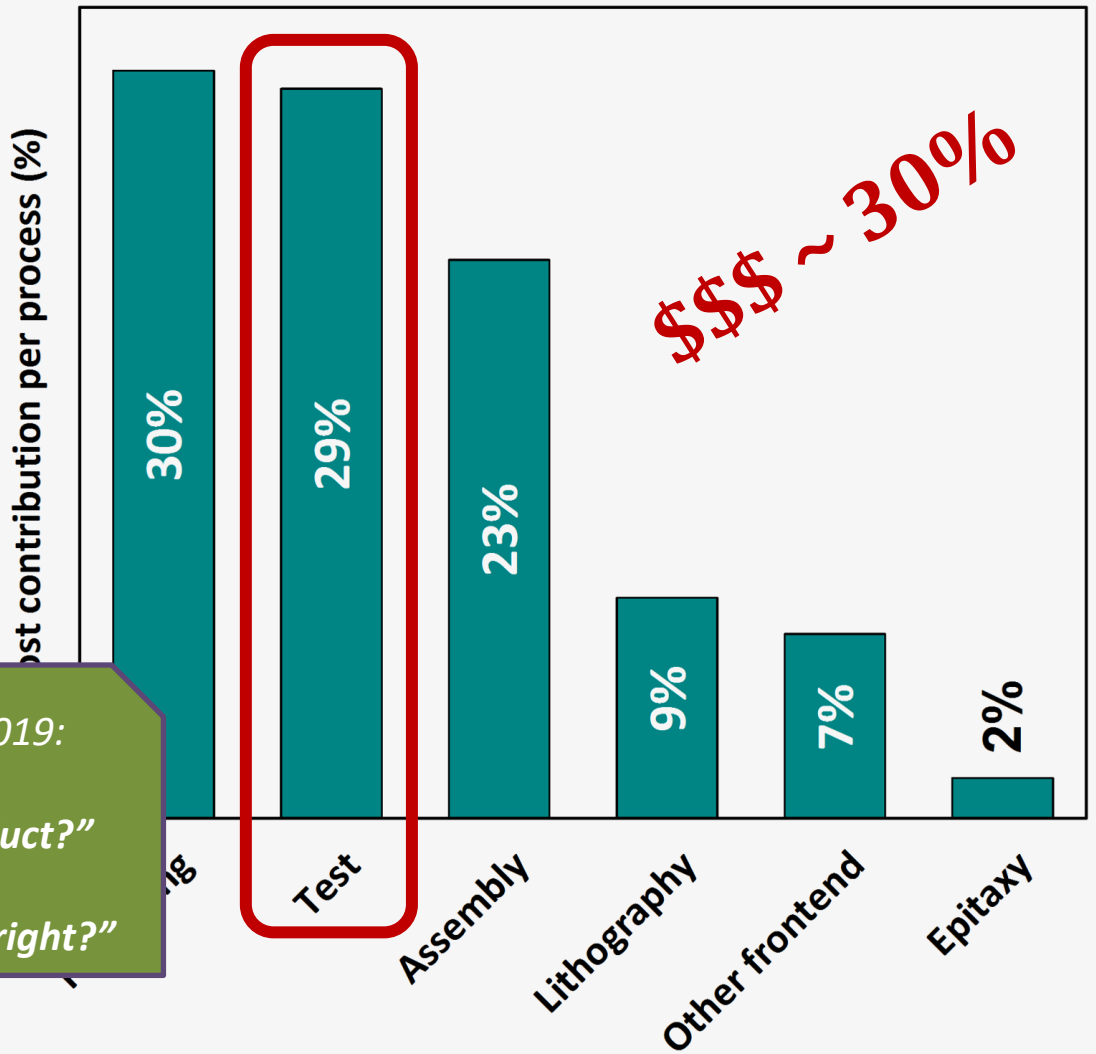

Chart based on data from a study of Erica R. H. Fuchs in IEEE JLT, vol. 24, No.8, 2006.

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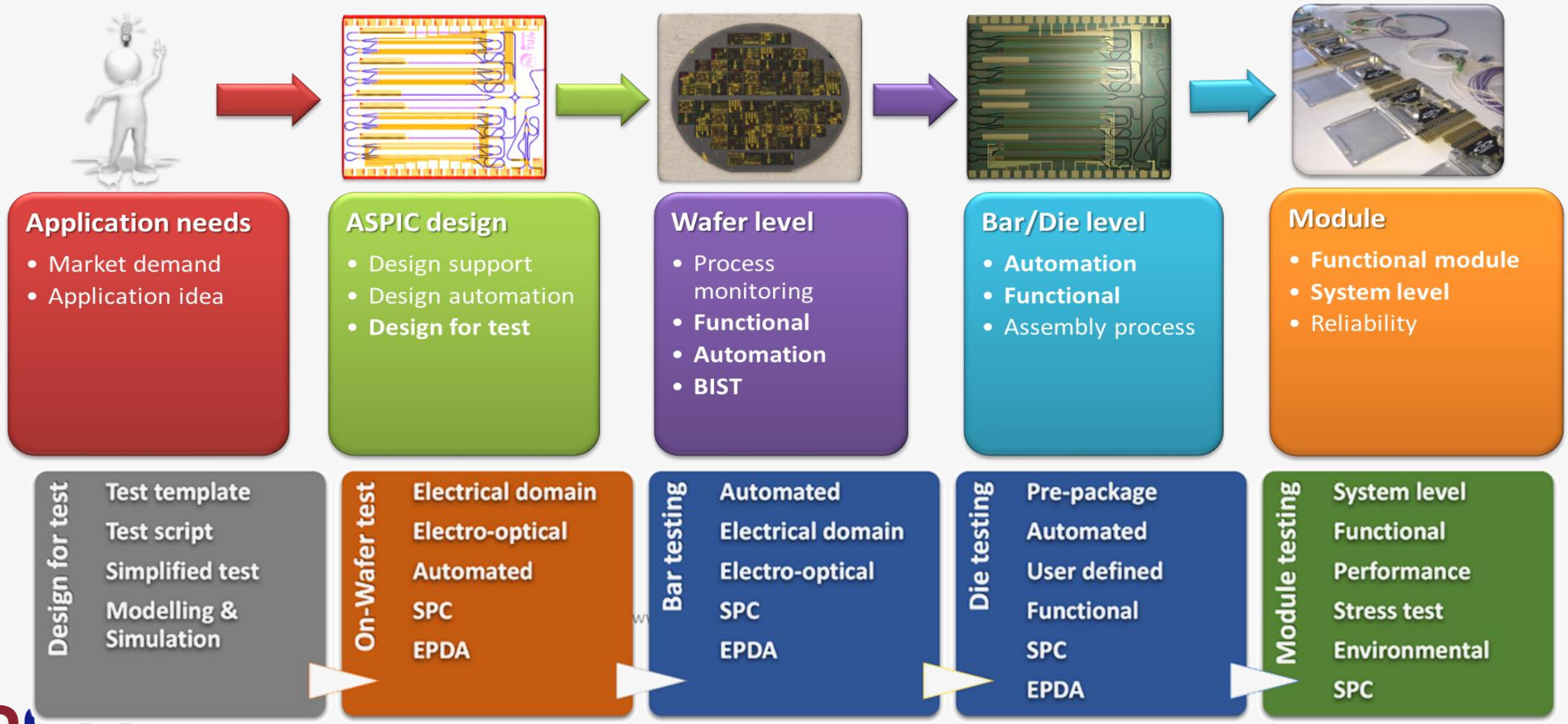
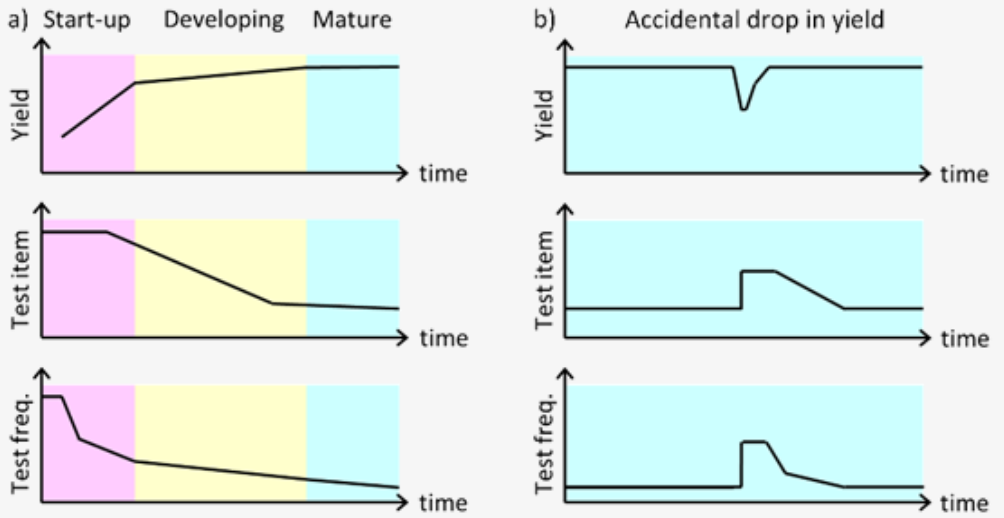
Test processes in PIC production chain



JePPIX Roadmap 2018 http://www.jeppix.eu/vision

Grand challenge: beauty & the beast

- **Characterization is a ‘beauty’**
  - Lots of data and information
  - Good for low volume, MPW,
  - Essential a ‘startup-phase’ of a product
  - **Resource demanding**
  - **Volume ‘unfriendly’**



Makoto Okano (AIST), Sylwester Latkowski(TU/e), IPSR-I 2019

- **Test is the ‘beast’**
  - **Needs to be swift (s/test = $$$)**
  - **Essential at early production stages (WLT)**
  - **A must for volumes**

‘Characterization ≠ Test’

Test processes in volume production of Integrated Photonics

- **Ideally as much as possible at wafer level (WLT)**
  - Electrical + optical
  - RF: available but is it essential here?
- **Highly automated**
  - Handling
  - Probing
- **Highly paralleled**
  - Multiple electrical and optical IOs (simultaneously)
  - Multiple-sites
- **Modular ATE**
  - Tools
  - Test equipment

'How much time ($) can be dedicated to test?'

Tests per second instead of test per minutes

' Number of IOs needed update'

5y – 10y -15y

~~20 -> 50 ->100~~ 256 -> 512 -> 1024

Dramatically reduced NRE and footprint

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WLT: Hybrid probe-cards

2023: Electrical-optical probe-card

- **Out of plane coupling e.g. gratings**
- Large MFD, alignment tolerant, **tens** of optical IOs
- DC + Optical
- Integration with AT (+1Y?)

'Such solution doesn't exist now and there seems to be a market for', Tobias

2028: Electrical optical probe-card NG

- **In-plane, edge coupling**
- **100+** optical IOs
- Small MFD, thither alignment accuracy
- DC+RF Optical

'Grating couplers… ehm', Martin & Sylwester

' SiPh folks eventually want them too', Makoto

2033: Optical solder bumps

- **1000+ optical IOs**
- Mixed signals
- Test and assembly suitable (flip-chip?)

How and when we will get 1000+ optical IOs?

'Optical Solder bumps' - *IPSR-I Winter 2019, Tokyo*

2040 should be OK…

"I'll be quite advanced in age' then, Ignazio

'Let feel like in SF movie, you all heard John E', Sylwester

"We've all seen Vanguard/KIT PHBs' so there is something, Martin

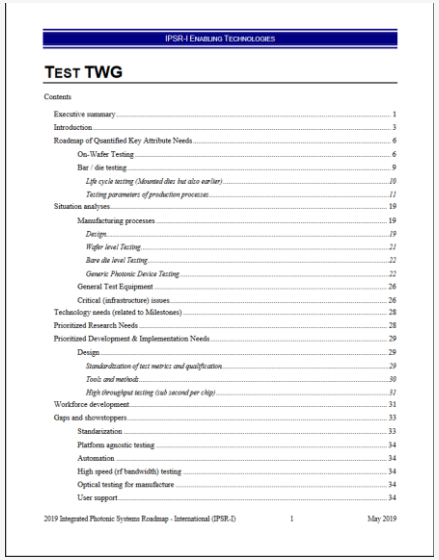
2030 we will have some!

Disclaimer: The quotes on the right are based on the loose notes of Sylwester from one of the TWG meetings ~2019-2020.

BIST: Built-In-Self-Test

2025: On-chip diagnostics

- Temperature monitoring
- Open, short CKT



2030: Self-calibration

- Parameter monitoring e.g. temp, power, lambda
- Feedback + correction signal
- Somewhat increased El Ph integration would help

2040: Re-purpose, Adaptive operation modes

- Failure-prevention
- Efficiency management e.g. Energy saving vs Performance
- Adaptive countermeasures
- Advanced logic needed -> Advanced (digital) El-Ph co-integration will be needed

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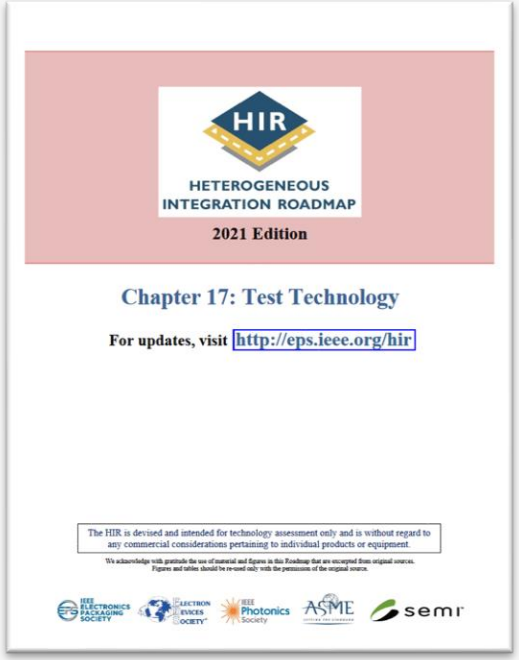
Testing of Photonics in Global Technology Roadmaps

- **Integrated Photonics Systems Roadmap – International 2020 (IPSR-I)**
  - AIM Photonics Academy and PhotonDelta
  - Electronic-Photonic Test and other chapters with a strong input from **PIXAPP and JePPIX**
  - https://photonicsmanufacturing.org/sites/default/files/documents/test.pdf



- **Heterogeneous Integration Roadmap 2021**
  - IEEE Electronics Packaging Society, Electron Devices Society, IEEE Photonics Society, American Society of Mechanical Engineers (ASME), SEMI
  - Chapter 17: Test Technology, Photonic Devices
  - https://eps.ieee.org/images/files/HIR_2021/ch17_test_final.pdf

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From technology roadmap to industry standards

- **IEEE Standards Association Photonics Committee (2019)**
  - IPSR-I Study Group (SG) to identify standardization potential
- **IEEE SA Project approval request (PAR)**
  - Output from **PIXAPP, JePPIX Pilot Line and OpenPICS** published at **openEPDA.org** serves as the base
  - SG drafts and submits the first PAR (Q3 2021)
- **Project approved by IEEE SA (December 2021) Project Number: P3112**
  - Title: **Standard for Electronic Photonic Design Automation – Open Data Formats – Terminology and Definitions**
  - Purpose: *The purpose of this standard is to unify data formats and exchange methods used in the photonic integrated circuits supply chain*
  - Need: *(…) fragmentation of the supply chain in the absence of any standardization efforts leads to inefficient product creation flows, long design-in windows, moderate yields at component and product levels, and elevated costs (…) A standardized approach will benefit fragmented PIC supply chain, vertically integrated businesses, original equipment manufacturers (OEMs), and automated test equipment (ATE) vendors.*

IEEE Advancing Technology for Humanity

IEEE SA STANDARDS ASSOCIATION

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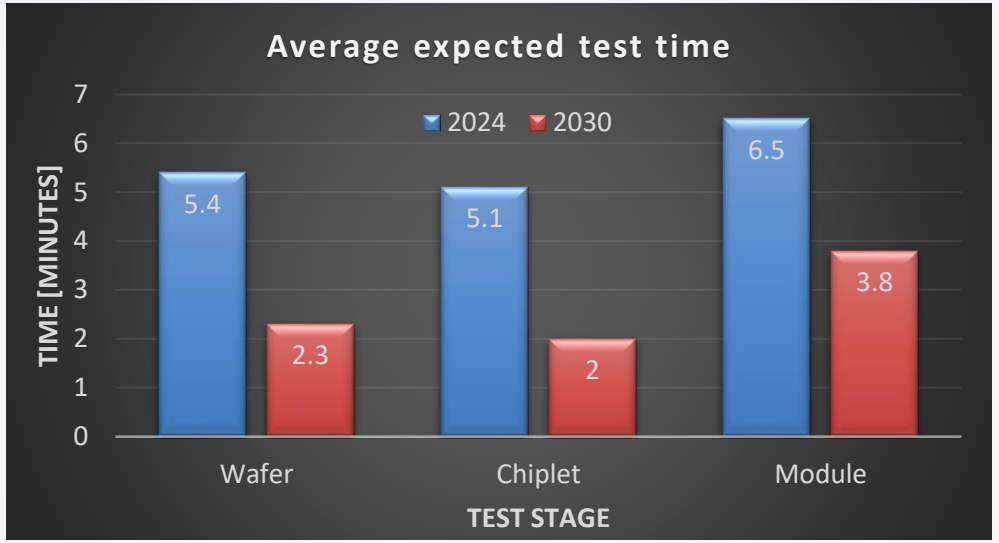
IPSR-I 2024 Sneak peek

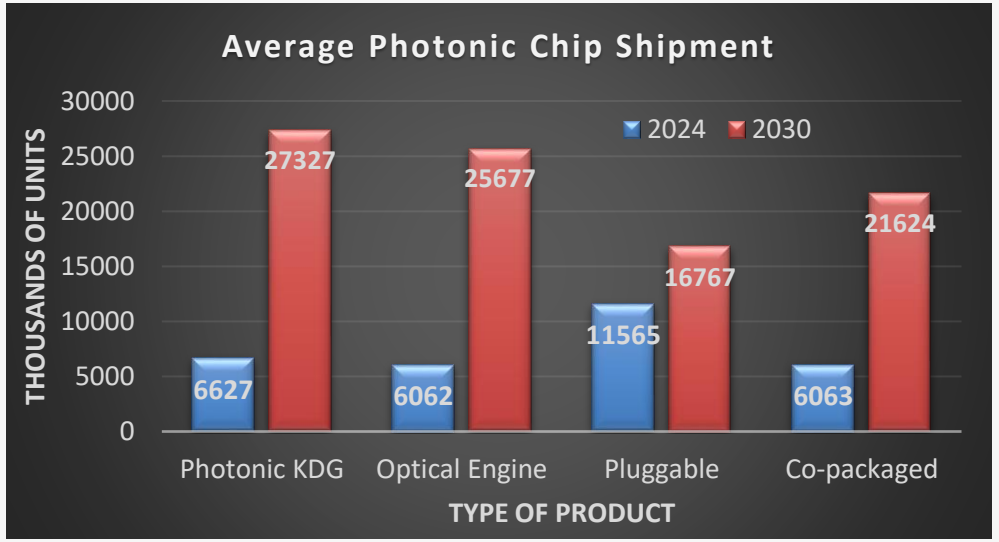
Electronic Photonic Test Chapter

- (More) Compact
- Re-Structured
- New input and data
- Industry-enriched content
- In your hands soon

Survey 2024 early preview *

- Expected test time
  - Minutes in 2024
  - 52% reduction in the next 5 years
- Expected product shipment
  - Millions (aggregated) in 2024
  - 300% increase in the next 5 years





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* Conclusions and plots are an initial take of one of the chairs. Subject to changes and approval of Test TWG chairs and changes in the published version

Photonic Integration Technology Center

- Joint Innovation Center on Integrated Photonics
- Accelerate the industrial uptake of integrated photonics
- Access to state-of-the-art photonic chip fabrication and integration facilities
- From application requirements to full system design to chip design and material and equipment development
- Organizing and executing complex and disruptive innovations with and along the value chain
- Shared Research Programs aligned with Industrial needs

PhotonDelta
Gateway to Integrated Photonics

TNO innovation for life

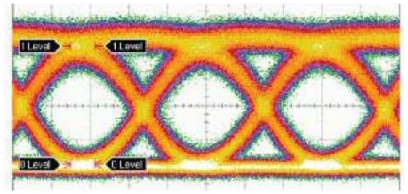
TU/e EINDHOVEN UNIVERSITY OF TECHNOLOGY

UNIVERSITY OF TWENTE.

Metrology Program

Objectives and strategy

- Product development cycles **reduced by at least 3 months**
- Development of **design-for-test** methodologies
- Next-generation characterization tools and methods to support **new product developments**
  - E-O bandwidth test at **+100GHz**, reproducible and fast linewidth/stability measurements with **>10measurements/second**
  - Polarization resolved test and characterization e.g., **degree of rejection >30dB**
- Advance and mature test throughput of test **from mins/device** towards **seconds/device**
- **Massively parallel testing** for production using automated and modular test equipment
- **Throughput ramp up by 10X:** from small-batch testing, extrapolate accurate models to minimize the overall number of test sites/device
- **Talent development** shaping dedicated training programs and contribute qualified workforce for the expected **5000 photonics related positions available by 2025**



PITC Metrology Program
launching partners

SALLAND Engineering
Test Technology Center

SMART PHOTONICS

PHOTONFIRST
Integrated Photonics Sensing

PITC
Photonic Integration Technology Center

BRIGHT Integrated PHOTONICS

Fontys
University of Applied Sciences

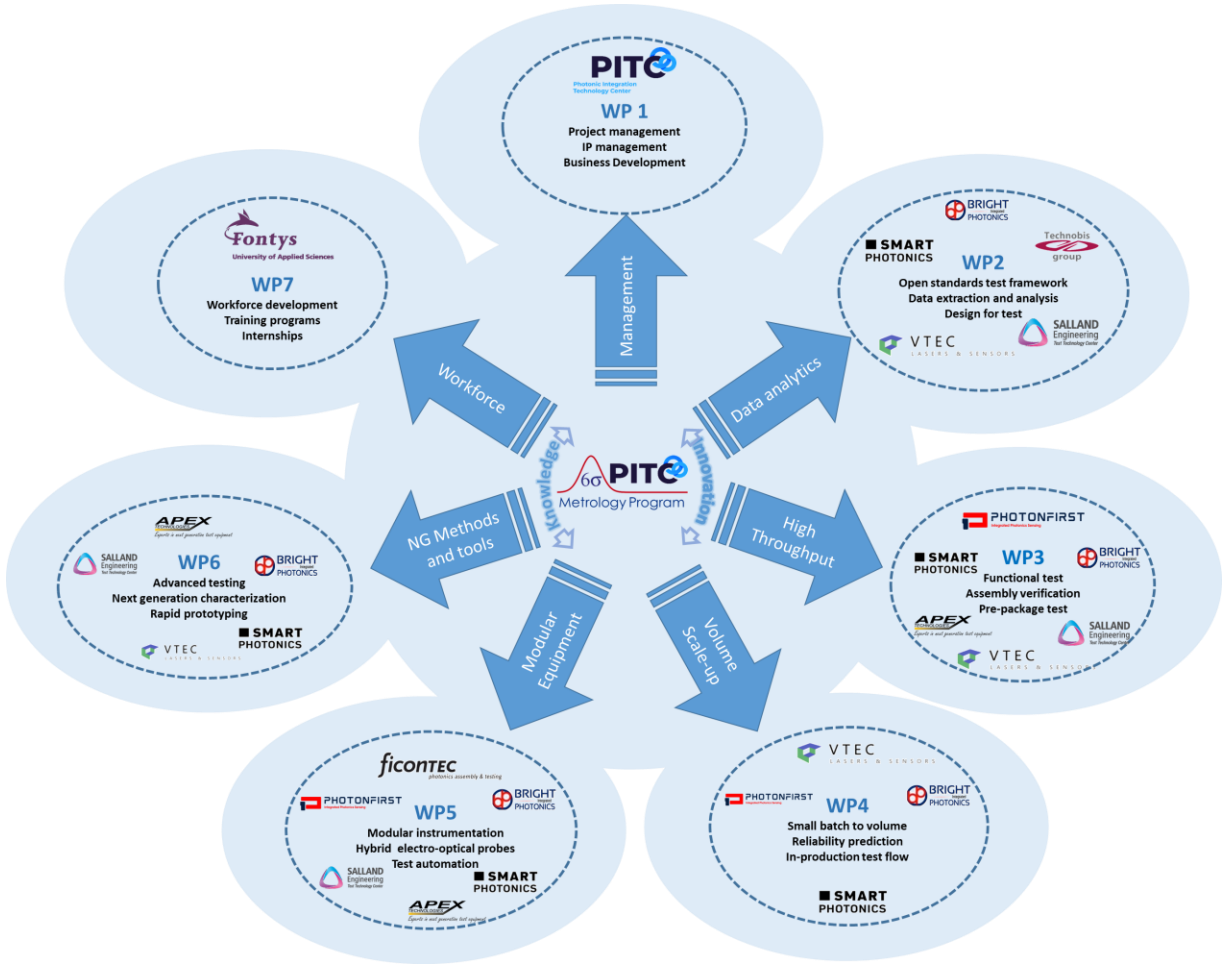
APEX TECHNOLOGIES
Experts in next generation test equipment

ficonTEC
photonics assembly & testing

VTEC
LASERS & SENSORS

Metrology Program
Technical agenda overview

Work packages	
WP1	Program management and business development
WP2	Data Analytics
WP3	High throughput testing
WP4	Test in small batch to volume scale-up
WP5	Modular tools and instrumentation
WP6	Next generation test and characterization
WP7	Talent development



Thank you!

Questions?

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Credits and sources:

www.nature.com

raith.com

www.intel.com

Lionix International

SMART Photonics

Effect Photonics

NanolabNL

JePPIX

TU/e

WUR

gigalight.medium.com

Saxion

The Internet

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UFO Probe® Card
High-Volume test solution for PIC Wafer-Level Test

Jenoptik webinar 2024: “Just the right PIC” | Tobias Gnausch

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Photonics at Jenoptik

Jenoptik at a glance
A leading globally operating photonics group

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Key facts

1991	Year of foundation
>80	Represented in countries
>4,400	Employees worldwide

Villingen-Schwenningen, DE
Metrology

Berlin, DE
Semiconductor, medtech

Dresden, DE
Micro-optics, opto-electronics

Bayeux, FR
Metrology

Monheim, DE
Traffic safety equipment

Triptis, DE
Polymer optics, electronic packaging

Rochester Hills, MI
Automation solutions, smart manufacturing

Freemont, CA
Application Center

Huntsville, AL
Micro-optics

Jupiter, FL
Optics, opto-electronics

Pyeontgaek, KR
Laser technology

Shanghai, CN
Optics, opto-electronics

Headquarter and place of foundation

Location

Organizational structure of the Jenoptik Group: Two photonics-based divisions and automotive business

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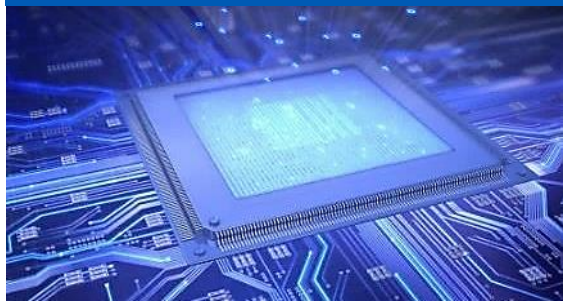
Advanced Photonic Solutions Division

Semiconductor & Electronics



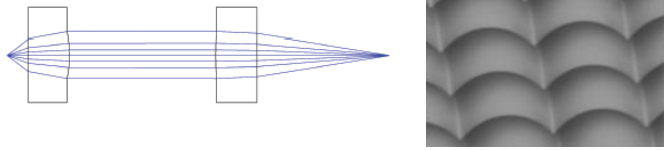
Optics, micro-optics
Precision components
Equipment for measuring and testing optics (gold standard)

Life Science & Medical Technology

Diode lasers
Microscope cameras
Imaging solutions
Optical components

ICT

Optical Coupling



Optical Wafer-level Test

Smart Mobility Solutions Division

Smart Mobility

Equipment for traffic surveillance
Software
Service to full operation

Non-Photonic Portfolio Companies

Automation systems and process solutions
Automated plant concepts

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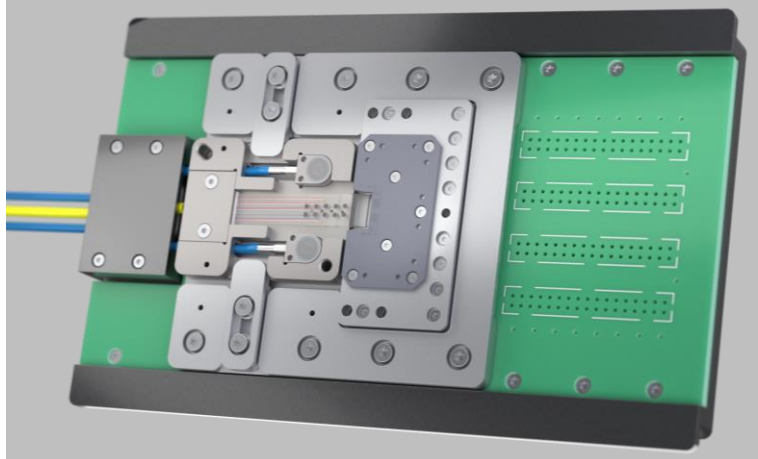


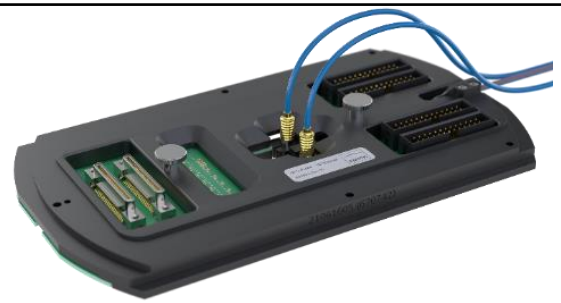
UFO Probe® Card
High-Volume test solution for PIC Wafer-Level Test

UFO Probe® Card
Enables High-volume Wafer Level Tests of Photonic Integrated Circuits (PICs)

JENOPTIK's High-Volume test solution for PIC Wafer-Level Test

- **Focus:** High-Volume Manufacturing Eco-system
- **Simultaneous** optical and electrical probing enables utilization of **existing IC test eco-system**
- **Cooperation** with probe card manufacturer and tester companies

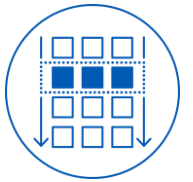
Courtesy of Sicoya



Simultaneous electrical and optical testing

Plug & Play for existing standard IC wafer probers

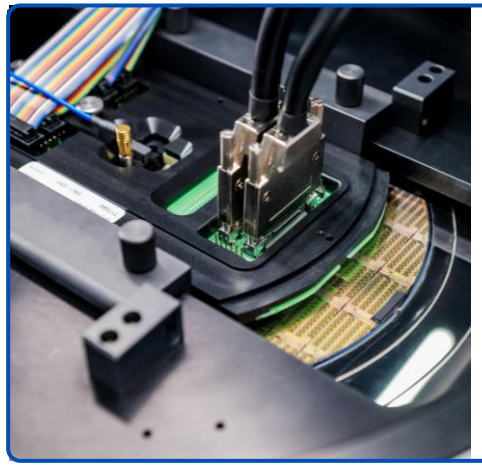
No active alignment time per chip



Parallel qualification of multi-DUT

Enables testing of more and smaller structures on chips

Integration



Runs on Standard IC wafer probers

Courtesy of Accretech

Plug & Play

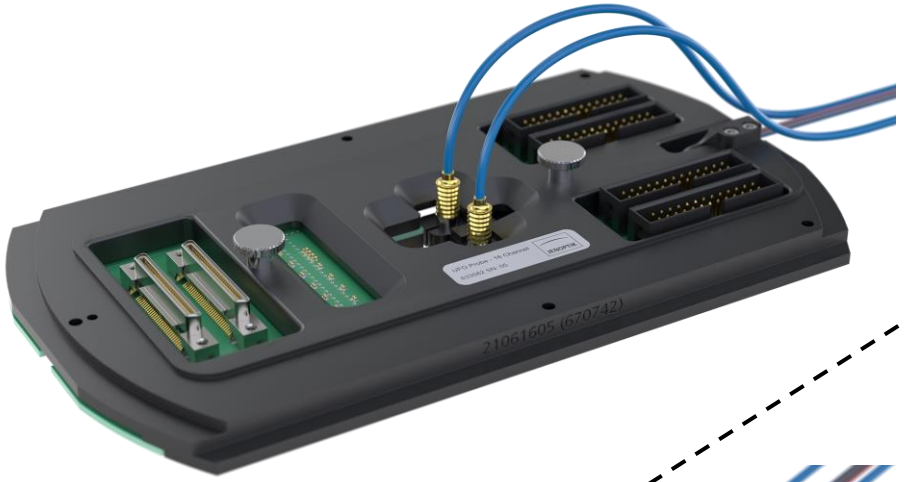
Design for **streamlined ATE integration**

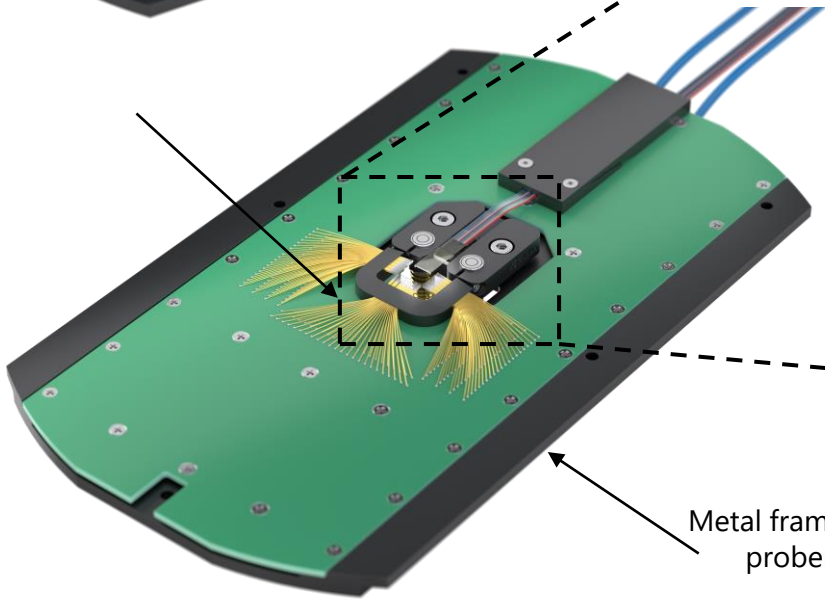
Courtesy of Advantest

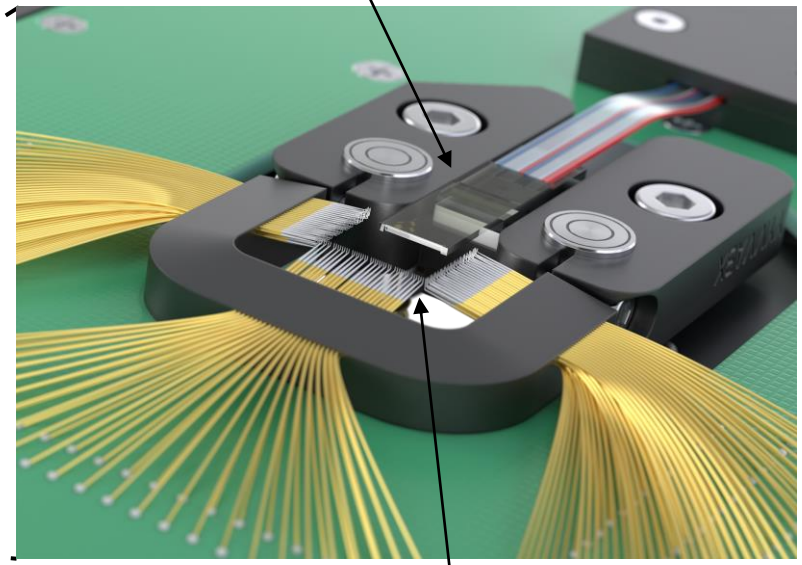
UFO Probe® Card
Enables High-volume Wafer Level Tests of Photonic Integrated Circuits (PICs)

Probe card key figures

- Standard prober interfaces
- **Monolithic optical module** with up to 32 channel
- Alignment insensitive optical coupling for **vertical emitting PICs**
- Simultaneous optical and electrical probing
- Utilize **proven needle technology** (partnering with probe card manufacturer)







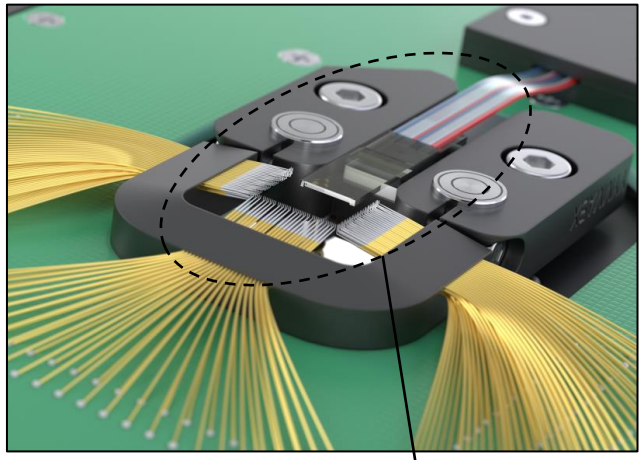
Monolithic optical module

Cantilever needle setup as electrical interface to the DUT

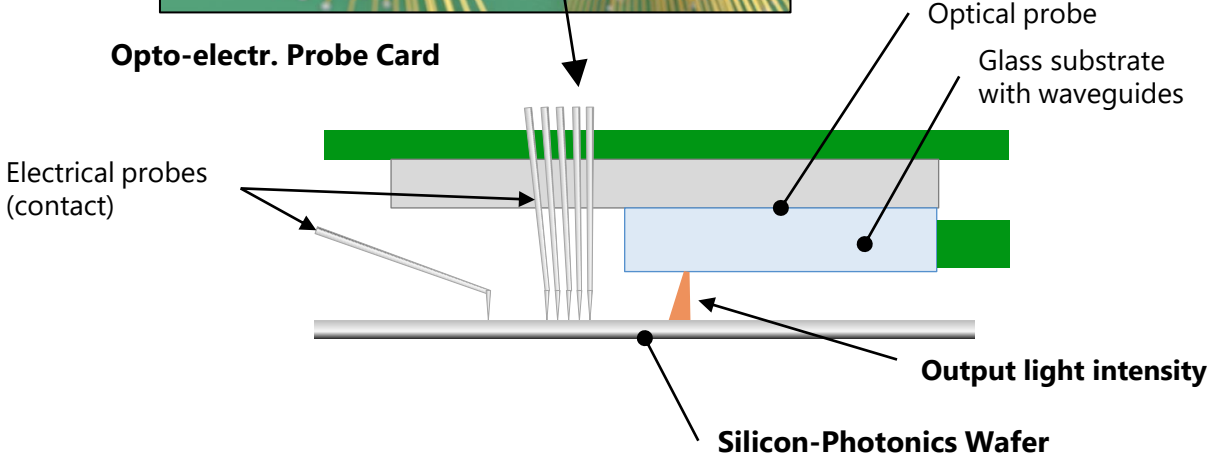
Metal frame as interface to prober head plate

UFO Probe® Card
Working Principle

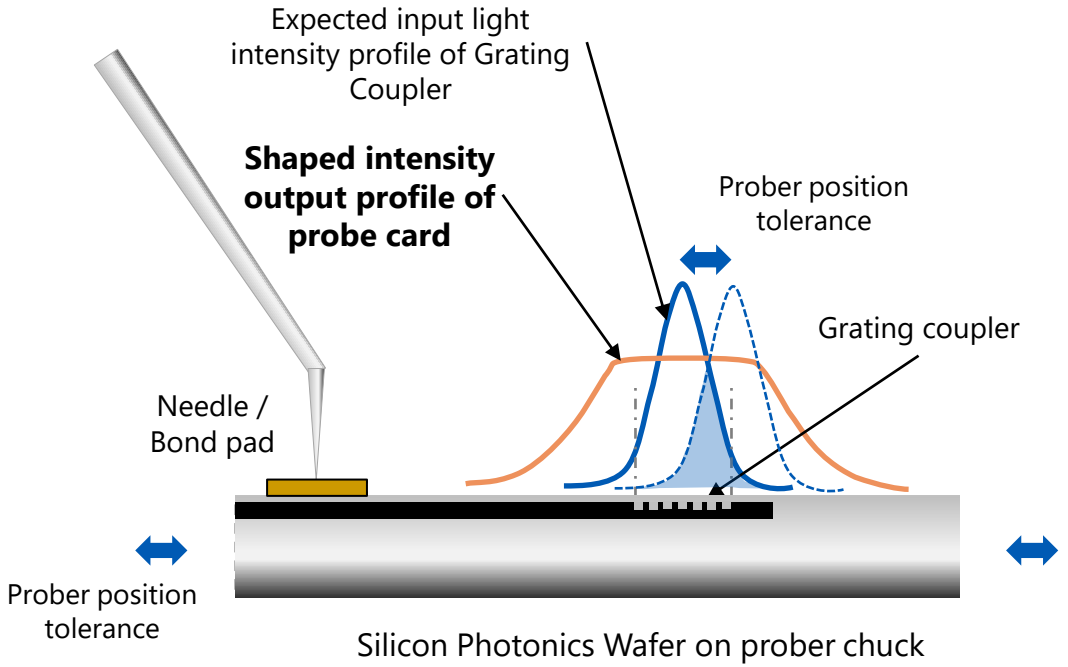
Alignment insensitive test solution for PIC Wafer-Level Test



Opto-electr. Probe Card



Optical concept compensates prober alignment tolerances.



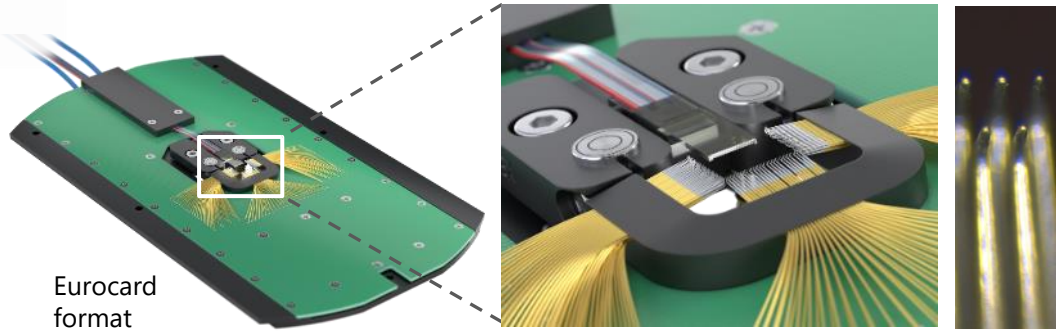
UFO Probe® Card
Probe card types

UFO Probe® Cantilever

- Works for **vertical emitting** PICs
- **Monolithic optical module** with up to 32 optical channels
- Optical standard pitch of **127µm and 250µm or individual pitch**
- **Cantilever** needle technology: ≤250 needles, pointed or flat tip
- Prober interface: Eurocard format
- Capacitive distance sensor for direct height control

Cantilever

Time saving simultaneous optical and electrical probing



Test solution

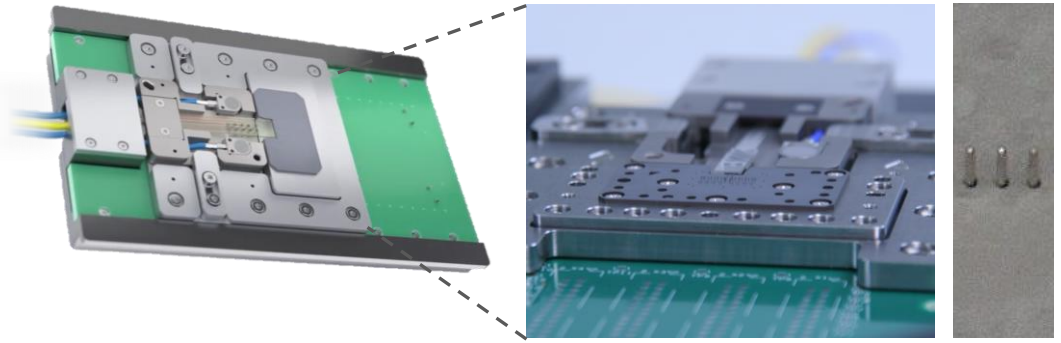
UFO Probe® Card
Probe card types

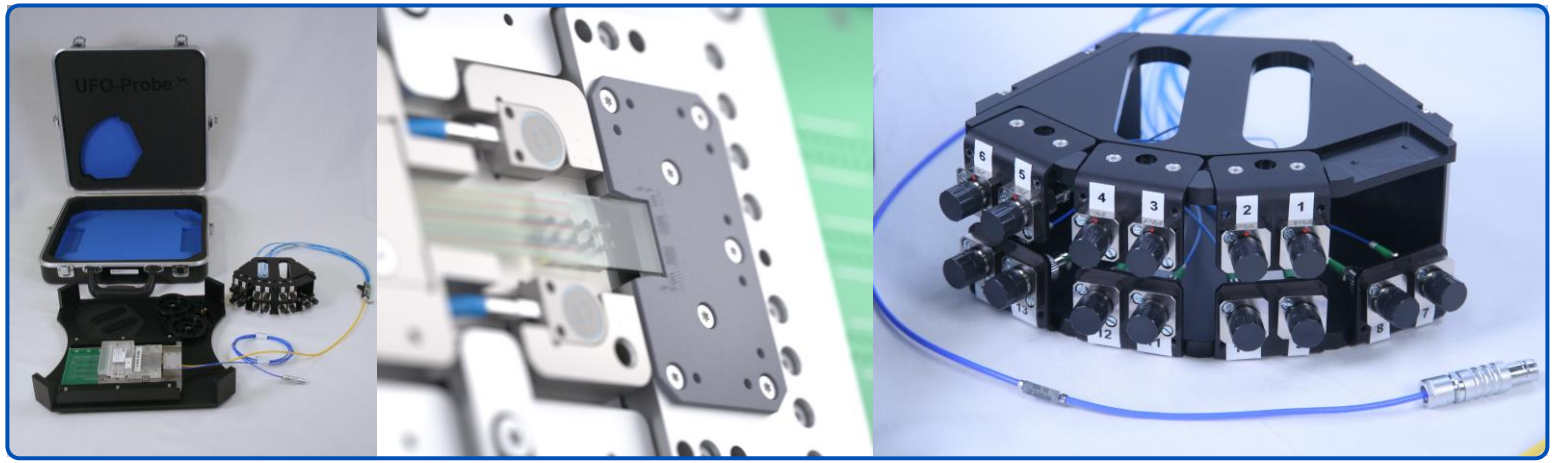
UFO Probe® Vertical

- For **small pad sizes** down to 35µm (square).
- Small needle pitch: ≥ 40µm
- **High needle count**: up to 30000 or more,
- Pointed or flat needle tip (pad and bump probing)
- Optical Channels: up to 32 or more, @ 1260-1630nm
- Improved fiber management
- **Multi-DUT** and **High frequency (RF)** capable
- Best choice for ATE usage

Vertical

High pin count and fine pitch probing





UFO Probe® Card
Further developments

UFO Probe® ATE

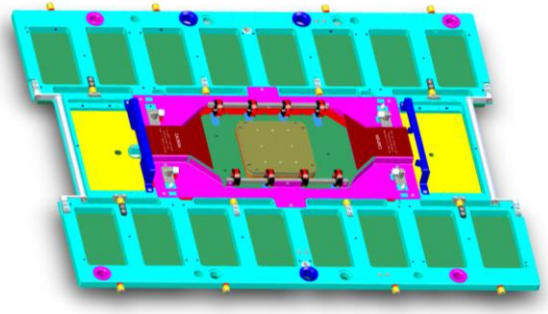
- Integration for direct docking ATE systems
- UFO Probe Technology for **vertical emitting PIC** test
- Path to high count optical I/O and multi-site

Optical connections

- PM-fibers and Multi-fiber connectors (also in combination)

Tester operability

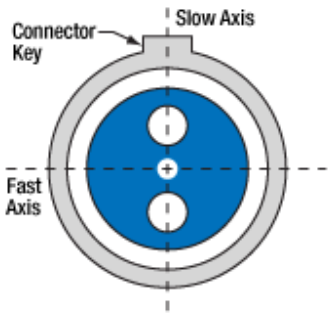
Ongoing joint efforts with Advantest for **streamlined ATE integration**

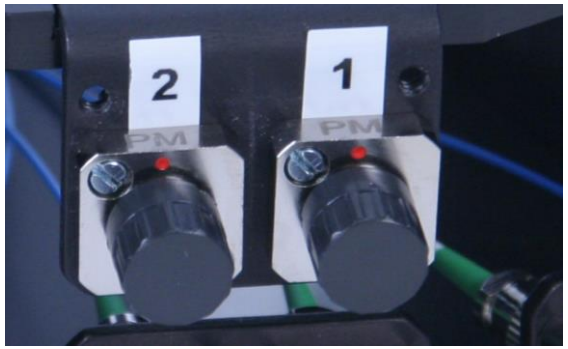


Courtesy of Advantest

Optical connection

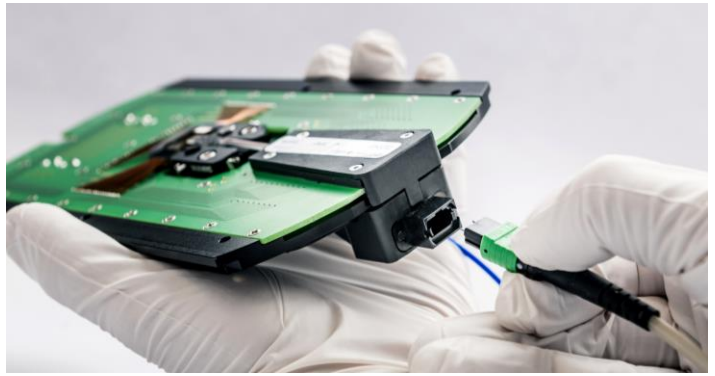
Polarization maintaining fibers



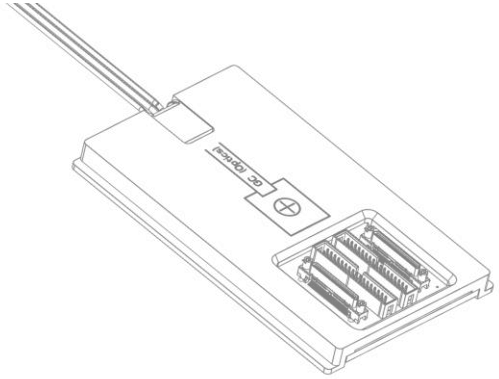


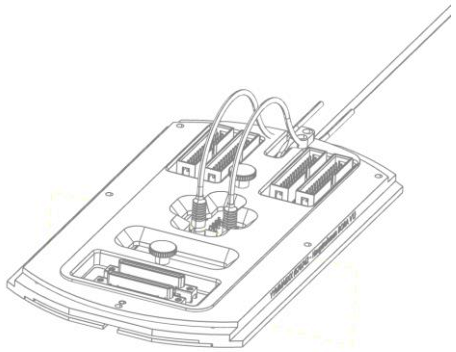
Optical connection

Multi-fiber connectors



UFO Probe® Card
Overview





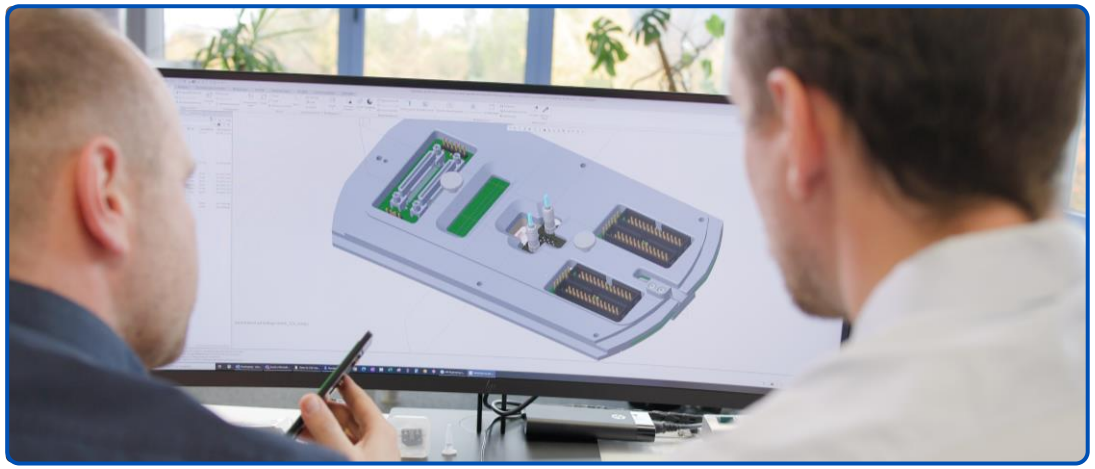
Specifications	Current generation	Future generations
Component to be tested (Device under test/DUT)	Electronic and photonic integrated circuits (EPIC); optical transceivers for data transmission and telecommunications applications	EPICs for transceivers, photodiodes, biosensors and Solid State LIDAR
Electric needle technology	Cantilever and Vertical	Cantilever, Vertical/Advanced
Optical coupling principle DUT	Vertical coupling	Vertical coupling
Number of optical inputs/outputs (OI/OO)	Up to 32 or more	<200
Pitch OI/OO	127 µm, 250 µm, flexible for >250 µm	flexible
Layout configuration of OI/OO arrays	Linear arrangement with same direction of inputs/outputs	Configurable to own needs
Coupling angle	0° and 11.6° standard, up to 20° customized	0° - 20°
Supported wavelength	1260 – 1625 nm (O/ L-band)	VIS to NIR (U-band)
Measurement of insertion loss	Repeatability: ~ 0.3 dB	Repeatability target: 0.1 dB
RF measurement	Up to 110 GHz, depending on needle technology	GHz
Number of PICs measured in parallel	One	Multi-DUT
Interfaces	Eurocard, ATE*	Eurocard, ATE full direct docking

* Currently without automatic optical docking

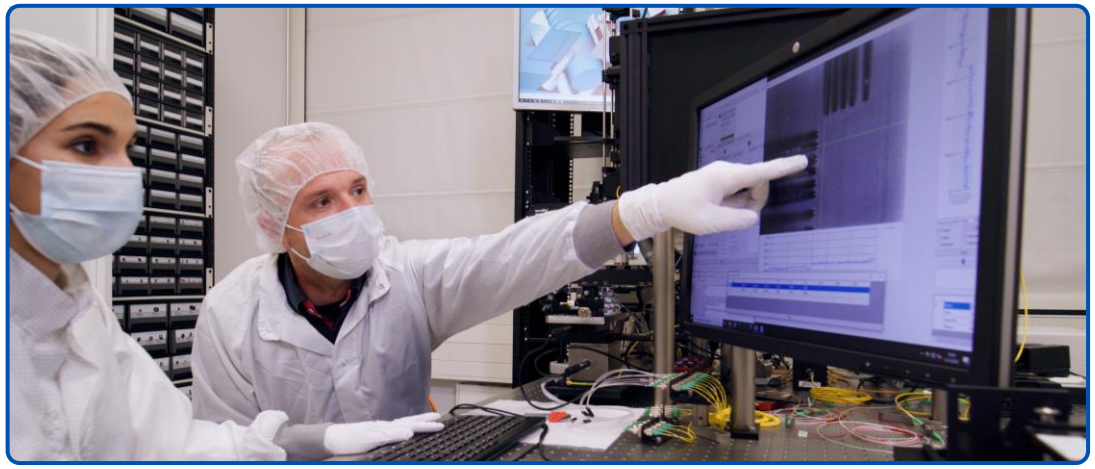
UFO Probe® Card
Jenoptik Competencies

- Design: Optical module and general E/O-probe card
- Manufacturing and supply chain
- Micro-assembly and alignment of optical and electrical modules
- Optical test and verification in lab: customized test rig
- Test under manufacturing conditions: UF3000 Prober

Innovation



Manufacturing



Verification

UFO Probe® Card
Jenoptik Competencies

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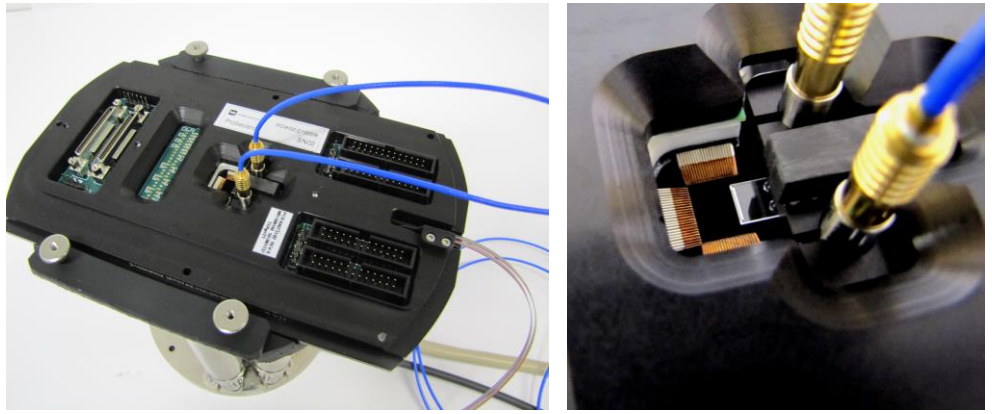
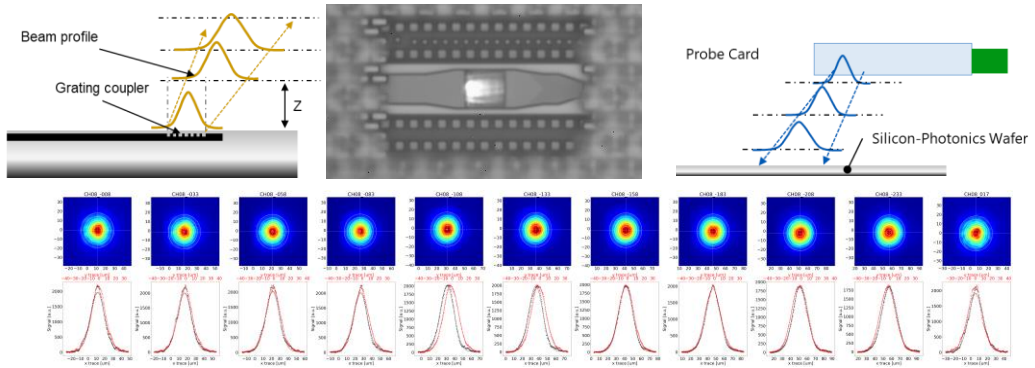
Innovation



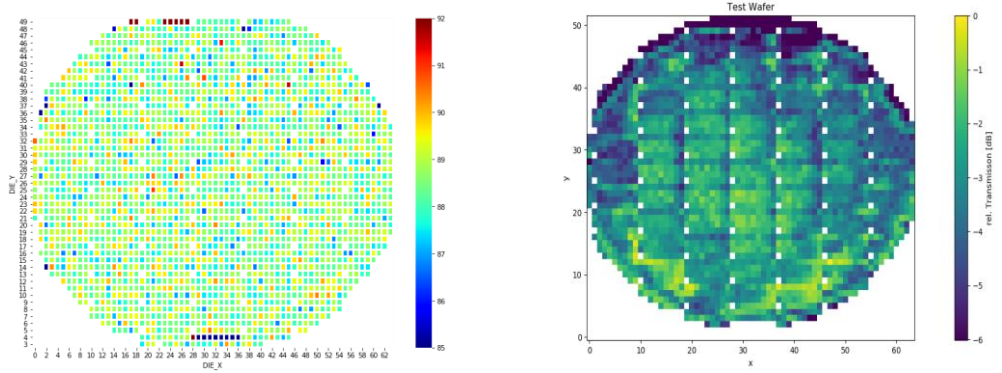
Manufacturing

Beam profile measurements



Verification

Wafer map generation and test measurements



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